A Novel Way of LTPS Model Extraction with Hysteresis and Transient Current Analysis


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Abstract
Time-sampling measurements are used in this paper to build time dependent LTPS TFT current model. The device model that considers bias and time dependent threshold voltage (Vth) shift and mobility degradation is implemented in Eldo through GUDM for simulating a pixel circuit as an indicator of panel performance.

Author Keywords
time-sampling measurement, LTPS, Vth shift, mobility degradation, Eldo, GUDM, transient current.

1. Objective and Background
The performance of a low-temperature poly-silicon (LTPS) thin film transistor (TFT) is usually judged by its threshold voltage (Vth), mobility (μ), sub-threshold swing (SS) and on-off current ratio (I_on/I_off) [1][2][3]. The roots of the variences on those performance indices are mainly the charge trapped in gate insulator layer, insulator -LTPS interface, grain-boundary and inside the grains [4][5]. The density of trap of each type can be derived with different kind of measures including hysteresis, SS and low-high frequency measure [6]-[10]. In addition to the trap concentration, the activation energy of the traps should be noticed too[11]. Nonetheless, the activation energy of the traps is bias dependent [11]. Therefore, the factors for threshold voltage shift include the gate and drain bias can be expressed as $\Delta V_{th} = \Delta V_{th}(V_{gs}, V_{ds}, Time, Temp)$. Our goal is to extract the time and bias dependency factor of Vth shift from I–V and time sampling measure method. The objective of building this model is to enable designers to simulate the image retention time in AMOLED pixel circuit for panel performance estimation.

2. Results
A P-type LTPS TFT is fabricated with 120nm gate insulator layer and channel dimension of 30μm in length and 3 μm wide. The electrical characteristics were measured in ambient temperature (25°C).

When studying the image retention behavior, the chessboard pattern shown in Figure 1 is usually used to observe the image residual phenomenon which is the direct evidence of image retention and the criterion of the panels’ quality check. The panel is controlled to display chessboard image for a certain length of time and then switch to pure gray image to observe how long the residual images of previous chessboard image remains. For the pixels, the image change consists of two types of operations, which are white (L255) to gray (L128) and black (L0) to gray (L128). Two panels with different image retention time are selected as the target for examining the effectiveness of the proposed model extraction method. One of them has residual image that lasts 10 seconds, and that of the other lasts 120 seconds. On each panel, one TEG is selected to represent the I–V characteristics of all TFT in the panel. In the following paragraphs, the origins of the residual image will be analyzed and an analytical approach of deriving and extracting the model parameters with transient current will be presented.

![Figure 1. Residual image test samples](image-url)

For an AMOLED panel, the luminance is from the OLED device whose current is controlled by the driving TFT. Therefore, we will focus on the variations of the LTPS TFT because the behavior variations of OLED are within milliseconds and is far from the scale of retention time observed [12]. To mimic the stability of the driving TFT current on a
The difference in green lines after switching to L128. Nonetheless, the threshold voltage shift decreases larger than \( V_{th0} \) because of larger vertical electric field. The threshold voltage shift decreases from \( V_{th0}^{white} \) to \( V_{th0}^{gray} \) after operation changes from L255 to L128. This phenomenon is called quasi-trapping because the charges which were trapped during operation L255 are de-trapped (recovery) instead of trapping when TFT device is on. This recovered threshold voltage shift \( \Delta V_{th} \) is in agreement with stretched-exponential equation either and can be expressed as

\[
\Delta V_{th} = \Delta V_{th0}' \cdot e^{-\left(\frac{t}{\tau'}\right)^{\beta'}} + \Delta V_{th0}^{gray}
\]

where \( \Delta V_{th0}'^{gray} = \Delta V_{th0}^{white} - \Delta V_{th0}^{gray} \), \( \tau' \) represents the recovered characteristic trapping time constant and \( \beta' \) is the stretched-exponential exponent. The time dependent current of TFT operating at L255 is similar to equation (1) but approaching the target value in different direction:

\[
\Delta I_{ds}(t) = \Delta I_{ds}'^{gray} - \Delta I_{ds}'^{gray} \cdot e^{-\left(\frac{t}{\tau'}\right)^{\beta'}}
\]

where \( \Delta I_{ds}'^{gray} \) is the Ids at infinite time with constant bias. At the moment that TFT operation enters L128, the difference between ideal and real current is

\[
\Delta I_{ds} \propto (V_{gray} - (V_{thi} + \Delta V_{th0}^{gray})) \cdot \Delta V_{th0}^{gray}
\]

The measured transient current data are then used to extract the coefficients in trapping and quasi-trapping behaviors including \( \tau, \beta, \beta' \) and \( \beta' \), whose values are listed in Table 2.

**Table 2.** Extracted coefficients for the driving TFT in trapping/quasi-trapping

<table>
<thead>
<tr>
<th></th>
<th>( \Delta I_{ds} )</th>
<th>( \tau )</th>
<th>( \beta )</th>
<th>( \Delta I_{ds}' )</th>
<th>( \tau' )</th>
<th>( \beta' )</th>
</tr>
</thead>
<tbody>
<tr>
<td>TEG 1</td>
<td>2.3e-8</td>
<td>1.3e-9</td>
<td>7</td>
<td>0.25</td>
<td>1.5e-9</td>
<td>20</td>
</tr>
<tr>
<td>TEG 2</td>
<td>2.8e-8</td>
<td>3.6e-9</td>
<td>100</td>
<td>0.28</td>
<td>3.9e-9</td>
<td>50</td>
</tr>
</tbody>
</table>

Figure 3 shows the measured transient current of both TEGs versus the calculated current with parameters in Table 2 and equations (1) to (5) which are perfectly matched with each other.
Although the non-ideality of TFT current can be explained with threshold voltage shift, it is not enough to explain the observation that we have on the panels because $V_{th}$ variation, either from process variation or charge trapping, is usually compensated with circuits and controls [4][15][16], as what is included in the panels (e.g. 6T-1C pixel circuit) that we used for observation. And yet, residual images with different retention time are still commonly observable. Therefore, we need to introduce more factors to explain the image retention phenomenon in display panel beyond considering the $V_{th}$ variation of TFT device. As explained in previous paragraphs, threshold voltage stability is caused by charge trapping, not only in gate insulator, but also in active layer too. When a charge is trapped in active layer, it affects the threshold voltage and mobility of the carrier simultaneously because the mobility is a function of gate bias, thermal voltage and threshold voltage [17]. The relation between effective saturation mobility ($\mu_{FEET}$) and the drain current of the TFT can be expressed as

$$\kappa \equiv \frac{d(I_{dsat})}{d(V_{gs})} \propto \sqrt{\mu_{FEET}}.$$  \hspace{1cm} (6)

where $I_{dsat}$ is the saturation drain current of TFT and $\kappa$ is the mobility related coefficient. To understand the mobility variation after bias stress, we use a multi-cycle DC stress measurement method in which the device is repeatedly measured after stress with different voltage. To be exactly, the value of drain-source voltage is fixed at -1.6V and the gate-source voltages applied at the TEG is in a sequence with the order of L0, L0, L128, L255, L255, L128 and L128 under 300 seconds for each. Since the conditions of these two TEGs are different, the operation of them in the designated level requires different voltages as listed in Table 3:

<table>
<thead>
<tr>
<th>TEG 1 (V)</th>
<th>L0</th>
<th>L0</th>
<th>L128</th>
<th>L128</th>
<th>L255</th>
<th>L255</th>
<th>L128</th>
<th>L128</th>
</tr>
</thead>
<tbody>
<tr>
<td>Initial</td>
<td>-0.2</td>
<td>-0.2</td>
<td>-1.0</td>
<td>-1.0</td>
<td>-1.4</td>
<td>-1.4</td>
<td>-1.0</td>
<td>-1.0</td>
</tr>
<tr>
<td>L128</td>
<td>-0.2</td>
<td>-0.2</td>
<td>-1.4</td>
<td>-1.4</td>
<td>-1.8</td>
<td>-1.8</td>
<td>-1.4</td>
<td>-1.4</td>
</tr>
</tbody>
</table>

With the bias change after each stress interval, the values of the mobility related coefficient $\kappa$ for both TEGs are calculated by using equation (6) and listed in Table 4.

<table>
<thead>
<tr>
<th>Initial</th>
<th>L0</th>
<th>L128_0</th>
<th>L255</th>
<th>L128_1</th>
<th>Delta</th>
</tr>
</thead>
</table>

For each measure, although the stress conditions are different, the values of coefficient $\kappa$ for L128 should eventually converge to the same value. Based on the equation (6) and Table 4, the mobility related coefficient $\kappa$ is an important indicator for image retention behavior observation. According to the coefficient $\kappa$ calculation results in Table 4, the value difference of $\kappa$ between two L128 operations in TEG 1 is smaller than the one in TEG 2. As a result, the observed residual image of TEG 1 which is from panel 1 that has 10 retention time is smaller than that of TEG 2, the one from panel 2 whose retention time is longer than 120 seconds. The relation between mobility degradation and threshold voltage shift are obvious because when charges are trapped in active layer, carriers will have a harder time to move through and thereby a degradation of mobility is observed. The implementation of the coefficients to translate threshold voltage shift to mobility degradation is implemented in the model we have built but the discussion of it is left as future work to be done.

### 3. Impact

In this paper, we utilized transient-Id measure with selected gate-source biases to extract the coefficients for threshold voltage shift equation that explains the current degradation of panels without threshold voltage compensation. We also use the multi-cycle DC stressed Id-Vg to witness the mobility changes under different stress condition to explain the retention time difference in a panel that includes a threshold voltage compensation mechanism. The parameter extraction for threshold voltage shift equation and mobility degradation equation are provided by in the extraction tool TOME from Legend Design Technology Inc. The transient-Id measure and the serial DC stressed Id-Vg measure can be used at the same time for the extraction and building of the model. This model is then implemented by as a plug-in device through Mentor Graphics’ GUDM and ELDO for simulating a 6T1C pixel to estimate the image retention time as an important indicator AMOLED panel performance, of which the discussion for the result will be left as a future work to follow.
4. References


