Extraction and simulation with time dependent Vth shift model for IGZO panel

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Abstract (35~50 words)

The impact of stress effect to the performance of an IGZO panel is discussed in this paper. Depart from conventional method of observing the threshold voltage (V_{th}) shift, the time dependency of serial I_D-V_G test is included in building an accurate V_{th} shift model. The model can be used to simulate the IGZO TFT current change under fixed bias for aiding the circuit design and optimization.

Keyword: IGZO TFT, Model, V_{th} shift

Objective and Background

Since amorphous InGaZnO (a-IGZO) thin-film transistor (TFT) was introduced in 2004[1], its electrical characteristics have been broadly studied and it has been widely used in active matrix organic light emitting diode display (AMOLED) [2] due to its superior characteristics which include high field mobility, excellent transparency to light, good uniformity, and suitable for large area and low temperature fabrication. However, the IGZO TFT reliability issue which is related to bias stress, visible-light, and temperature are still not resolved. When IGZO TFT is under positive gate bias stress, positive threshold voltage (V_{th}) shift is induced by the electron which is trapped in gate insulator (GI) and/or GI/IGZO interfaces. While a large positive V_{GS} and positive V_{DS} are applied to IGZO TFT, the significant V_{th} shift degradation caused by self-heating and hot-carrier generation can be observed [3]. In addition to the constant gate and/or drain biases stresses, the remarkable impact of visible-light on the characteristics of IGZO TFT has been reported. The reliability of IGZO TFTs under the negative bias and illumination stress (NBIS) which is caused by the hole trapping in a GI and/or a GI/IGZO interface, the creation of ionized oxygen vacancies (V_o^+ or V_{o2}^+) [4], the donor-like defects in IGZO TFT channel, and electron trapping at a back channel interface [5][6] and the illuminated positive gate-bias stress which performs a superior stability than the dark stress [7] have been reported. Besides DC static stress studies of the IGZO TFT, the AC and dynamic stress behavior and mechanisms have been investigated recently [8][9] because the estimating

degradation behavior may not be correct for practical circuit designs when considering DC static bias stresses only. For a switching operation in a practical display driver circuit which is designed by IGZO TFTs, the degradation behavior under AC bias stress is dominated by the carrier trapping efficiency which provides different degradation behaviors under PBS and NBIS[8]. As reported in [9], the threshold voltage shift induced by frequency dependent dynamic stress in IGZO TFT increases when the stress frequency decreases. In the studies of threshold voltage shift, the temperature plays an important role because the amount of the generation of thermally activated carriers from traps in the band gap of IGZO TFT is temperature dependent. Recently, the temperature effect in IGZO TFT degradation has been extensively studied [12]. Based on our investigation, many studies have reported the gate-bias stress dependent instability according to the charge trapping/de-trapping model [13]. In this paper, we utilized the tool from Legend Design Technology Inc. to extract DC stressed I-V model including the threshold voltage shift under positive and negative bias stress, and use it to simulate the panel behavior to establish the ability of choosing or optimizing a circuit that will perform the best with a given process condition. It is very important for a designer to get the best profit from a handful of combinations of process variations and pixel designs.

Results

The IGZO TFT TEG used in this paper has gate insulator 310 nm-thick with relative permittivity 4.5, thin-film layer of 40nm-thick with relative permittivity 11.5, channel length 12μm and width 24 μm. The electrical characteristics were measured in ambient temperature 25^{o}C.

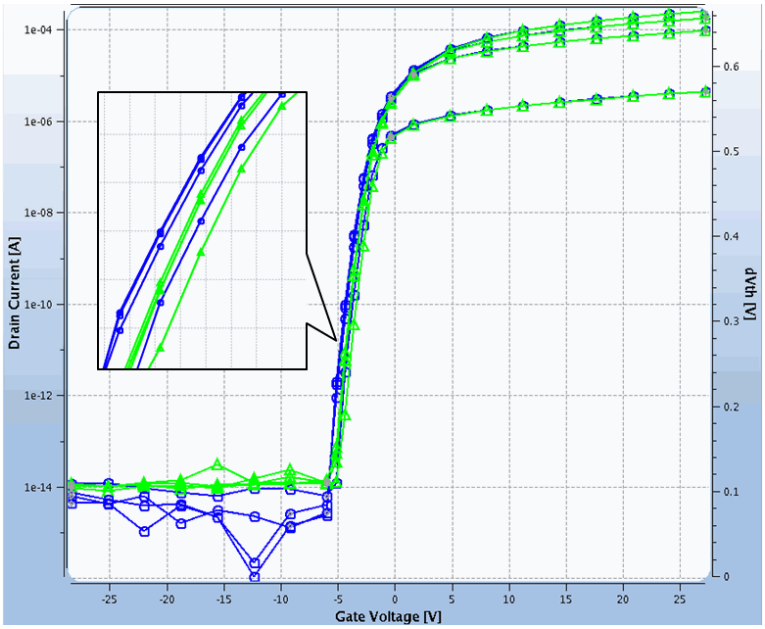


Figure 1: Initial I_D-V_G Measure with Various V_{DS} Bias

The TEG is biased at V_{DS} of 0.2V, 4.7V, 9.2V, and 13.7V. It is measured with V_{GS} from -30V to 30V, a.k.a. forward sweep, followed by a backward sweep, i.e. from 30V to -30V for V_{GS}. Inset of figure 1 shows that the threshold voltage is larger in backward sweep than that of forward sweep. It is usually refer to as the hysteresis of the IGZO TFT. To get a better understanding for the V_{th} relation among those measures, the V_{th} measurement results are shown in figure 2.

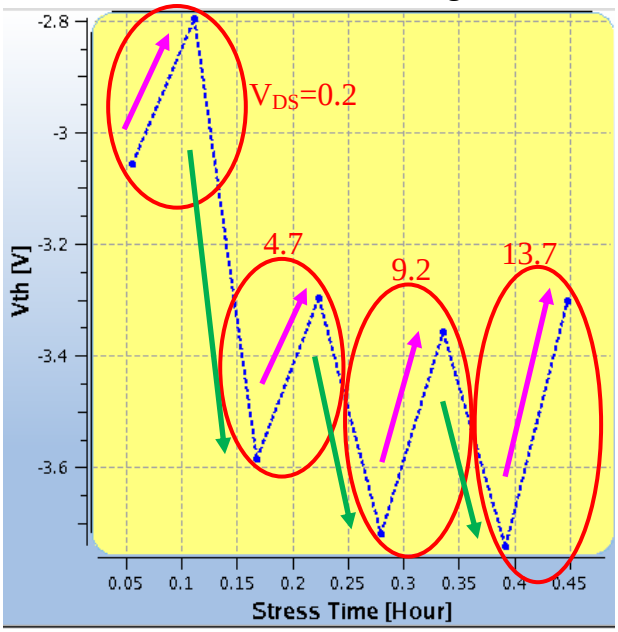


Figure 2: V_{th} plot in a set of I_D-V_G measure

The X-axis is the time spent for doing each I_D-V_G sweep and the Y-axis is the V_{th} value corresponding to each sweep. The circles in Figure 2 represent combinations of forward and backward sweep of I_D-V_G with various V_{DS} biases. The lower data point inside a circle is the V_{th} of forward sweep because it is known to be smaller than the one from backward sweep. The difference between them is the V_{th} increase due to charge trapping when the TEG is turned on. The amount of the V_{th} increase is calculated by summing the V_{th} increase at each V_{GS} bias and can be expressed as the extended-exponential equations [5][6][7][10]:

$$\Delta V_{th}^{increase} = \sum_{j=j\_on}^{j\_max} \Delta V_{th}^{trap}\left(V_{DS}, V_{GS_j}, \Delta V_{th}^{trap}\big|_{j-1}, \Delta t_j\right)$$

$$+ \sum_{k=k\_max}^{k\_on} \Delta V_{th}^{trap}\left(V_{DS}, V_{GS_j}, \Delta V_{th}^{trap}\big|_{k-1}, \Delta t_k\right)$$

where $\Delta V_{th}^{trap}\left(V_{DS}, V_{GS_j}, \Delta V_{th}|_{j-1}, \Delta t_j\right)$

$$= (V_{GS_j} - V_{th,j-1}^{trap}) \cdot \left\{ 1 - \exp[-(\Delta t_j / \tau_{V_{DS}}^{trap})^{\beta}] \right\}$$

j_on and k_on are the indexs of forward and backward as the TEG is starting to be turned on. j_max and k_max are the indexs of forward and backward as the TEG is biased on the maximum voltage. For j[th] time step (Δt_j), V_{GS_j} is the V_{GS} bias, $V_{th,j-1}^{trap}$ is the threshold voltage after (j-1)[th] step, β is the stretched-exponential exponent, and $\tau_{V_{DS}}^{trap}$ represents the characteristic trapping time of carriers with V_{DS} dependence [9].

The V_{th} difference between the backward sweep and the forward sweep of next V_{DS} bias is more complicated. It involves threshold voltage drop from charge de-trapping and the drain-induced-barrier-lowering (DIBL). By excluding the DIBL part, we can still express the difference with the following equation:

$$\Delta V_{th}^{decrease} = \sum_{j=j_{on}}^{j\_min} \Delta V_{th,j}^{detrap} \left(V_{DS}, V_{GS_j}, \Delta V_{th}^{detrap}\big|_{j-1}, \Delta t_j \right) + \sum_{k=k\_min}^{k_{on}} \Delta V_{th,k}^{detrap} \left(V_{DS}, V_{GS_j}, \Delta V_{th}^{detrap}\big|_{k-1}, \Delta t_k \right) \quad (2)$$

where $\Delta V_{th,j}^{detrap} \left(V_{DS}, V_{GS_j}, \Delta V_{th}^{detrap}\big|_{j-1}, \Delta t_j \right)$

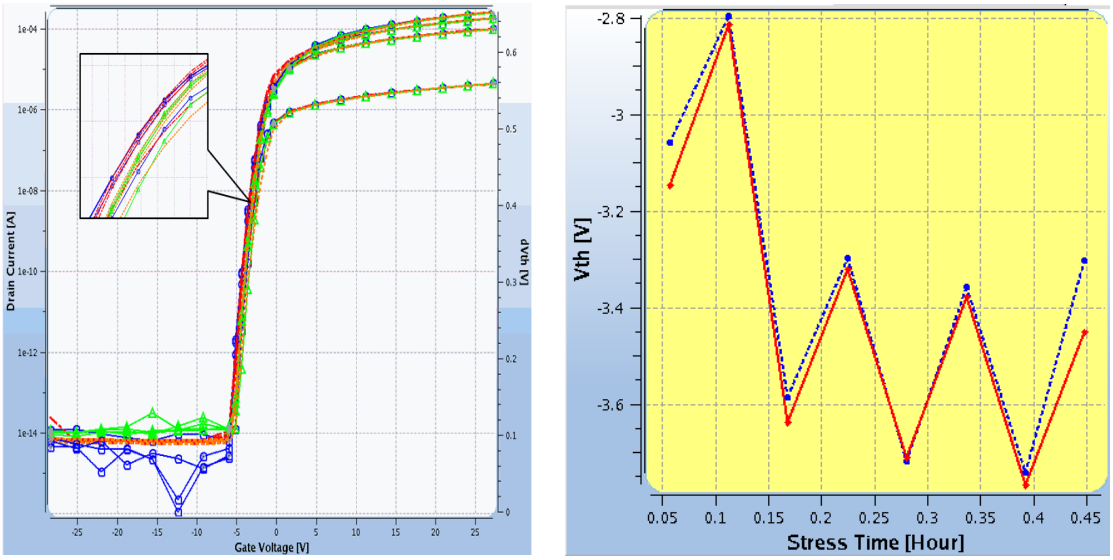
$$= \Delta V_{th,j}^{detrap-max}(V_{GS_j}) \cdot \exp[-(\Delta t_j / \tau_{V_{DS}}^{detrap}(V_{GS_j}))^{\beta}]$$

j_min and k_min are the indexs of forward and backward as the TEG is biased on the minimum voltage. For j[th] time step (Δt_j), V_{GS_j} is the V_{GS} bias, $\Delta V_{th,j}^{detrap-max}(V_{GS_j})$ is the maximum V_{th} shift before j[th] step and $\tau_{V_{DS}}^{detrap}(V_{GS_j})$ represents the characteristic de-trapping time of carriers with V_{DS} and V_{GS} dependence [7][9].

Linking equations (1) and (2) together with various V_{DS}, we can get the final V_{th} shift after a set of I_D-V_G measure with considering forward sweep, backward sweep, and various V_{DS} biases as:

$$\Delta V_{th\_set} = \sum_{all\ Vds} \left(\Delta V_{th}^{increase} + \Delta V_{th}^{decrease} \right) \quad (3)$$

For the equation above, there are coefficients for many arguments to be extracted to fit the measured I_D-V_G data and the V_{th} shift behavior at the same time. The result is shown in figure 3.



(a) A set of initial I_D-V_G (b) Extracted vs. Measured V_{th}

Figure 3: Extracted model vs. measured data for a set of initial I_D-V_G

The measurement of each V_{DS} bias took about 7 minutes, including forward and backward sweeps, which make the measurement for the whole set took 28 minutes for 4 different V_{DS} biases. Figure 3 shows the measurement results of the I_D-V_G current characteristics and the V_{th} shift after stress along with the model extraction results.

After the extraction of a set of I_D-V_G is done, the TEG is stressed under a certain DC bias for the observation of the stressed behavior. The threshold voltage under DC voltage stress is proposed by logarithmically equation dependent on the duration of the bias stress [11], and is rewritten here as:

$$\Delta V_t^{stress} = \gamma_0(V_{GS}, V_{DS}) \cdot \log(t/\tau_{V_{DS}}^{stress}) \quad (4)$$

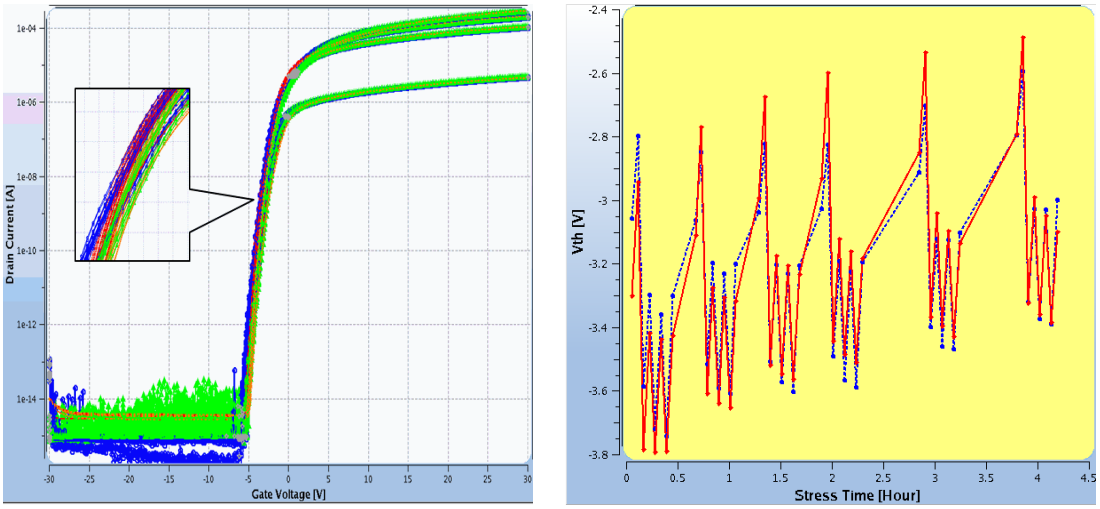
where $\gamma_0(V_{GS}, V_{DS})$ is a decay rate constant with V_{GS} and V_{DS} dependence. $\tau_{V_{DS}}^{stress}$ represents the characteristic stress time of carriers with V_{DS} dependence.

Concatenating V_{th} shift from DC stress, equation (4), and V_{th} shift from a set of I_D-V_G measure, equation (3), the V_{th} shift behavior of a DC stressed I_D-V_G measure can be obtained to match the V_{th} shift observed with the result as figure 4. The measurement and stress are done in the sequence listed in Table 1.

Operation	Duration(min)	Total(min)
Initial Set Id-Vg	28	28
DC Stress	10	38
Set Id-Vg	28	66
DC Stress	10	76
Set Id-Vg	28	104
DC Stress	10	114
Set Id-Vg	28	142
DC Stress	30	172
Set Id-Vg	28	200
DC Stress	30	230
Set Id-Vg	28	258

Table 1 : Time table of serial DC stressed I_D-V_G measure

Figure 4(a) shows that all I_D-V_G measure including initial, stressed, forward and backward are all properly extracted. Furthermore, figure 4(b) shows that the relation of V_{th} shift along the measure of each set of I_D-V_G and the stress period are all well fitted.



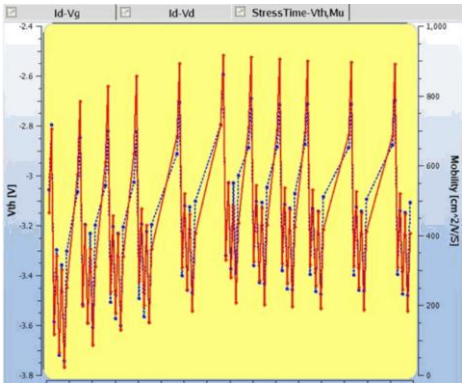
(a) Serial DC Stressed I_D-V_G (b) Extracted vs. Measured V_{th}

Figure 4: Extracted vs. measured V_{th} for serial DC Stressed I_D-V_G

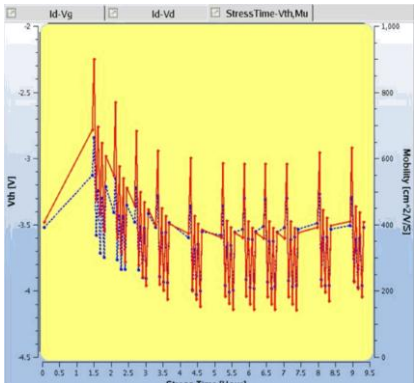
After the serial constant DC stressed I_D-V_G model is done, more data are included to further improve the model. The Table 2 lists the DC stress combinations that are used to stress the device and do the measurement.

	V_{GS1}	V_{GS2}
Sequence 1	Large Positive (30v)	Medium Positive (15v)
Sequence 2	Small Positive (5v)	Medium Positive (15v)
Sequence 3	Large Negative (-30v)	Medium Negative (-15v)
Sequence 4	Small Negative (-5v)	Medium Negative (-15v)

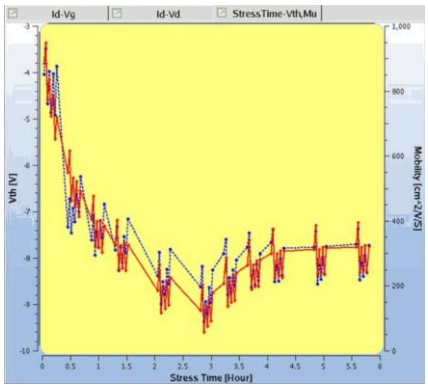
Table 2: Stress sequences with different V_{GS} combinations



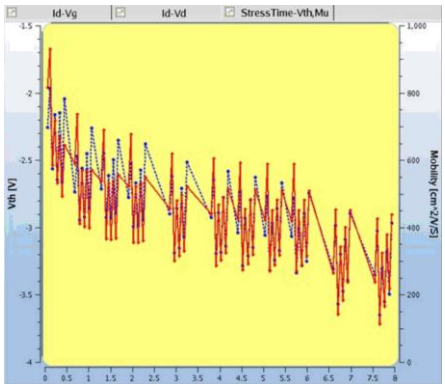
(a) 30V to 15V



(b) 5V to 15V



(c) -30V to -15V



(d) -5V to -15V

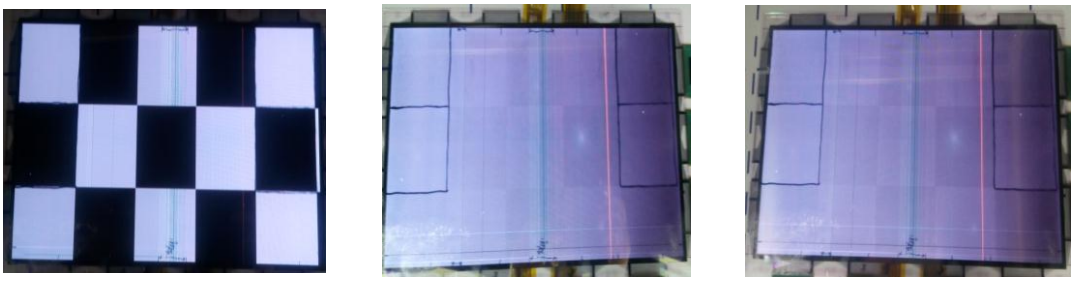
Figure 5: V_{th} shift vs. time for different stress sequence

From the measurement of variable DC stressed serial I_D-V_G measure, the V_{th} shift has the same sign as the stressing voltage. For figure 5(a), the stress voltage changes from 30V to 15V. It is supposed to have a large positive V_{th} shift and then a medium V_{th} shift. However, the time for 30V stress is not long enough to reach the maximum V_{th} shift for a 30V stress in the model, and that is why the V_{th} shift does not drop as quick as observed from the data. For figure 5(b), the device did not have a clean start because the trend for small positive stress should be going up instead of going down. So, an initial stress condition is added for doing the extraction. Figure 5(c) and 5(d) on the other hand are both having a correct trend that shows larger negative V_{th} shift under larger negative bias stress. The extracted results for negative V_{th} shift are thus relatively better comparing to the positive bias stress ones.

Impact

The time dependency of serial variable DC stressed V_{th} measure is included for the extraction of IGZO TFT model. With the time dependency, the V_{th} shift for the device can be extracted with the capability of simulating the current changing behavior that affects the quality and performance of an IGZO panel. Thereby, the proposed model should be a good indicator to help designing and optimizing a better panel. We have prepared some panel observation as the following figure to be

compared with the simulation result for the next step.



(a) Chess board image (b) Stressed 1H (c) Stressed 3H

Figure 6: Residual image test with different stress time

References

List a few main references covering projects in related areas.

To-be-added

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Prior Publications

There's no publication of ours prior to this submission.