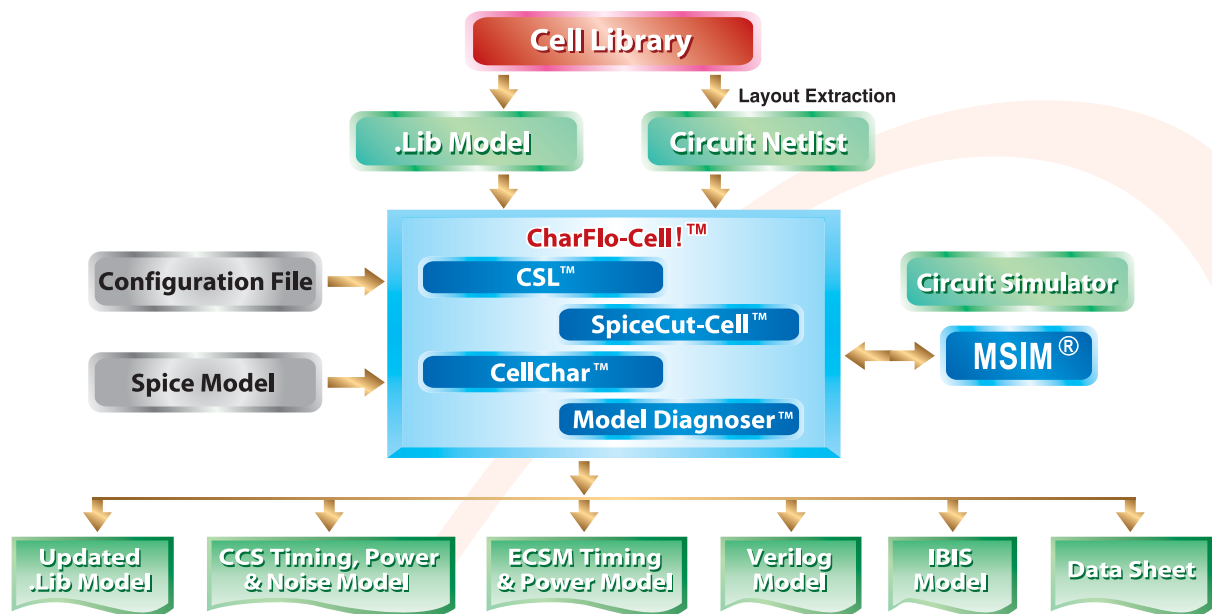


CharFlo-Cell!TM

Next-Generation Cell Library Characterization



CharFlo-Cell! is a next-generation standard cell and I/O library characterization product, designed mainly for reliability and manufacturability aware.

Characterization Flow

- **CSL**
Automate cell library characterization through programmable setup for '.Lib-in and .Lib-out'.
- **SpiceCut-Cell**
Analyze the inside of cells and locate internal nodes to watch for ensuring the modeling quality, and enabling complex I/O cell characterization.
- **CellChar**
Characterize standard cell and I/O library by using the multi-goals bi-section method.
- **Model Diagnoser**
Diagnose any .lib model at any PVT, and report signal-integrity problems or functional failures caused by that .lib model.

Manufacturability-Aware Models

- **Multi-goals Bi-Section Method**
Perform bi-section iterations based on multiple goals: output pins' function and internal nodes' signal integrity, to get the 'true' setup/hold time.

Inside Circuit Analysis

Execute circuit analysis inside the cell and check glitch, meta stability, signal noise and delay for modeling accuracy.

High-Throughput System

- **Fast Turn-Around Time (TAT)**
Optimize characterization process, remove the lengthy linear search, and take advantage of the fast inner-loop capabilities of circuit simulator.
- **Distributed processing**
Run concurrent simulation jobs distributed on server farms.

Automatic Setup for Easy Use

- **Stimulus generation**
Automatically generate input stimulus through cell's function, state-table and type, with the input states logically verified.
- **Control generation**
Automatically generate controls by inheriting from the existing .lib model, or by entering through Command Line Interface / Graphical User Interface.
- **Database generation**
Automatically generate database of results which can be flexibly accessed for creating library models in various formats, with the measurement results thoroughly validated.

Setup/Hold Time Characterization

• Conventional method I

Locate 'near function failure' setup/hold time using bi-section function in simulator. Then, through linear search, find 'target' setup/hold time which results in cell delay 5% more than the ideal one corresponding to the 'infinite' setup/hold time. The possible drawbacks are

- Slow performance due to linear search
- Inconsistent tabular results

• Conventional method II

Locate 'near function failure' setup/hold time using bi-section function in simulator. Then, add a margin to the 'near function failure' setup/hold time as the 'target' setup/hold time.

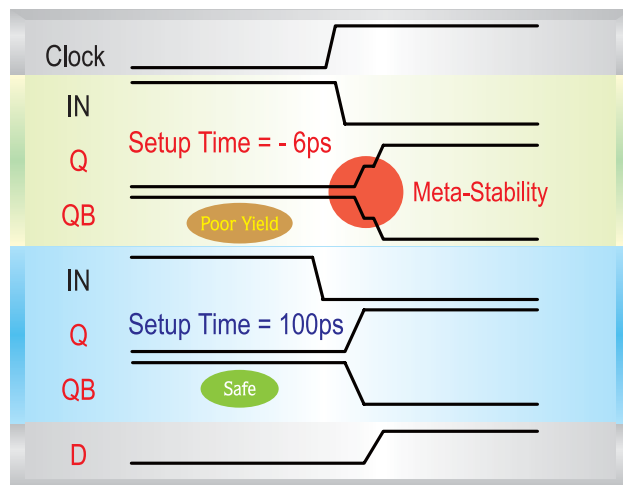
The possible drawbacks are

- Poor yields if 'not enough' margin
- Sacrifice performance if 'too much' margin

• Patented multi-goals Bi-Section method

Locate high-risk nodes inside the cell by using SpiceCut-Cell. Then, in addition to examining output-pins' switching correctly, CharFlo-Cell! makes sure there is no 'signal integrity' issues inside the cell during bi-section iterations. The benefits are

- Fast
- Accurate
- Consistent tabular results



Cell Types Supported

- Single and multi-output combinational cells
- Complex latches and flip-flops

- I/O pads and Tri-state cells
- I/O cells with multiple voltage supplies
- I/O cells with differential inputs/outputs and modal pins
- Special cells

Complex I/O Cell Characterization

- Customize the measurements intelligently.
- Renovate the algorithms for modeling complex interfaces with the board designs.
- Enhance the configurations for simulation convergence.
- Facilitate the measurements on internal node recognized by circuit pattern.

Model Diagnoser

- Locate 'easy-to-break' parts in .lib model of any cell library at any PVT.
- Report signal-integrity problems quantitatively, which are caused by the .lib model either incorrectly characterized or inappropriately applied at new PVTs.
- Identify the cells whose functions are inconsistent or whose input states are illegal.

Specification

Inputs

- Existing Liberty (.lib) models
- Layout-extracted cell netlists
- Spice models
- Configuration files

Outputs

- Updated Liberty (.lib) models
- Timing, power and noise models
- CCS and ECSM models
- SPDM table expansion, and monotonic modeling options
- Verilog models
- Report and Data Sheet

Platforms and Supports

• Computer Operating Systems

Sun Solaris, HP-UX and Linux (RedHat 7.3 and higher)

• Simulation Job Controls

SunGird and LSF

• Spice simulators supported

MSIM, HSPICE, and most commercial and in-house Spice simulators

Legend
Design Technology

www.LegendDesign.com
email:sales@LegendDesign.com

Legend Design Technology, Inc.
Headquarter
2880 Lakeside Drive, Suite #101, Santa Clara, CA 95054
Tel: +1 (408) 748-8888 Fax: +1 (408) 748-8988

Taiwan Office
5F., No.176, Sec. 2, Gongdaowu Rd., Hsinchu300, Taiwan, R.O.C.
Tel: (+886) 36 111 888 Fax: (+886) 36 111 889