Legend
Design Technology

CharFlo-Memory!™

The Complete Tool Set for Automatic Memory IP Verification and Characterization for SoC Designs

The CharFlo-Memory!™ Product Family

MSL™
MemChar SpiceCut Library, the tool for automating memory characterization with customized setup of '.Lib-in and .Lib-out'

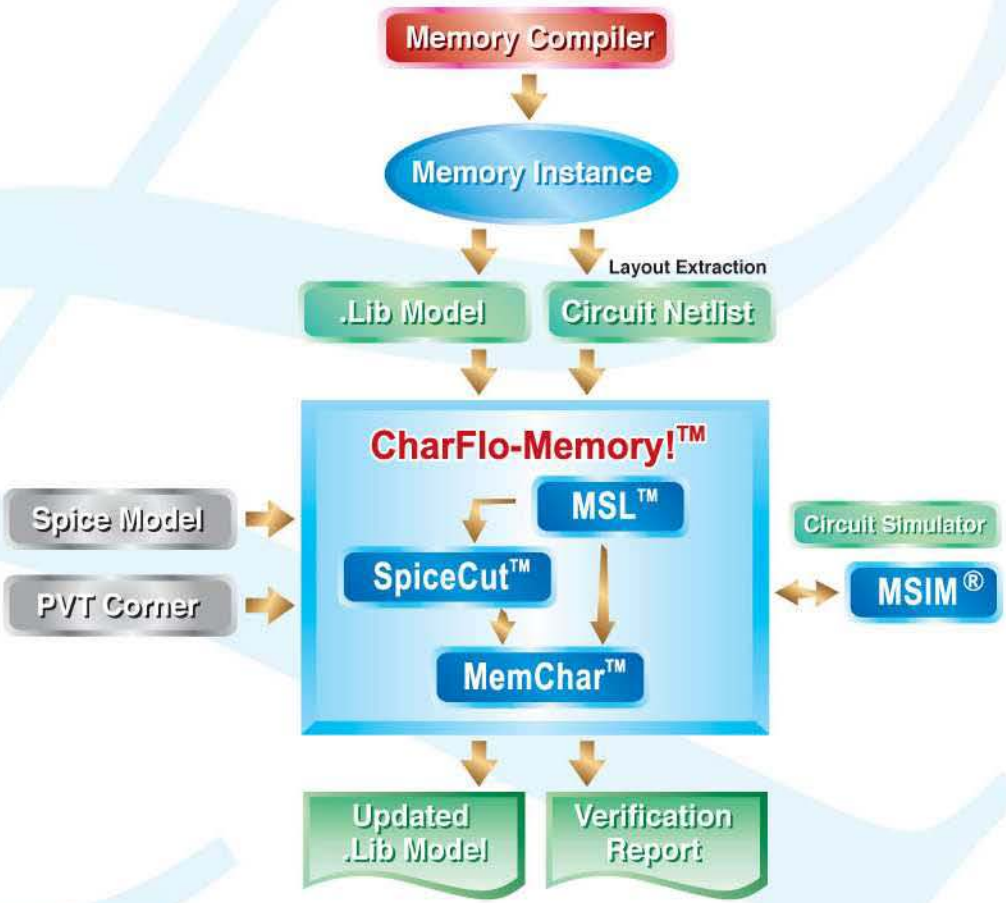
SpiceCut-Memory™
The tool for building critical-path circuits based on layout-extraction with RCs.

MemChar™
The memory characterization tool with optimization and reliability checking

MSIM®
The characterization-oriented circuit simulator.

Rethinking the way

CHARACTERIZATION is done



Overview

CharFlo-Memory! is an EDA toolset that enables engineers to characterize and verify memory IP automatically. The industry proven tools are used to ensure first-silicon success and high yield. For deep submicron designs (.18 and below) understanding the impact of second order effects - signal integrity, coupling, leakage power - on memory IP performance is crucial. Even for slower designs, if the signal is not latched correctly in the memory circuit poor silicon yield will result.

The CharFlo-Memory! toolset consists of MSL, SpiceCut, MemChar and MSIM. The tools provide the benefits of Accuracy, Throughput and Automation in Memory Characterization.

Applications

- Instance-based characterization for in-house and external memory IP
  - Memory compiler modeling development, including timing, power and capacitance etc.
  - Accurate instance model for low-power or high speed design
  - Re-targeting, e.g. 0.25um to 0.22um
  - Porting to multiple foundry sources
- What-if analysis
  - Process, Voltage and Temperature (PVT)
- Verification
  - Validation for QA and failure prevention
  - Spot-checking process revision
  - Debugging and failure analysis

Advantages

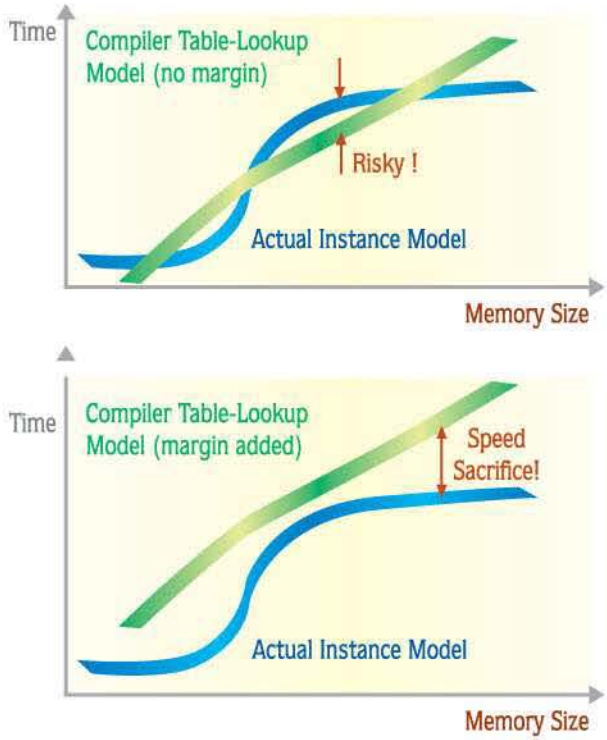
- Operate on layout-extracted circuits - preserving the silicon reality.
- Generate accurate on-chip instance model, instead of interpolating or extrapolating.
- Build optimized critical-path circuits automatically for high-throughput and simulation efficiency.
- Provide a complete solution with both bi-section and path-difference methods.
- Proven in production and silicon for numerous designs.
- Improve silicon yields by eliminating glitches and by performing margin checks.

Compiler vs. Instance Based Memory Models

Memory compilers can generate several hundred thousand different size instances. Since it is next to impossible to characterize each and every one, what is commonly done is that compiler providers characterize only the largest, the smallest, and selected cases in-between. The resulting compiler model is based upon interpolation and extrapolation from those original 'grid' characterizations

The interpolation error of the compiler's table-lookup model might represent the timing values as being less than actual silicon. This uncertainty can lead to failure or low yield.

Margin could then be added to the model for protection. However, the added margins might make the timing from compiler's table-lookup model slower than actual silicon. The performance is then sacrificed.



MSL: '.Lib-in and .Lib-out' Automation

With an emphasis on productivity and value, MSL is used to implement a push-button '.Lib-in and .Lib-out' characterization flow for compiler generated memories. For each memory instance, MSL reads in the compiler generated '.Lib' model, and automatically generates the control files for MemChar and SpiceCut needed to run characterization. MSL will update the '.Lib' model after characterization is complete.

Due to the variations of memory compiler designs, MSL will apply customized rules for generating the controls of MemChar, SpiceCut and for updating the '.Lib' file output. The customized rules constitute the MSL specification file for each memory compiler.

SpiceCut: Building Critical-Path Circuits

The netlist size of a layout-extracted memory instance can be enormous. This poses a major bottleneck for efficient characterization. Therefore, building critical-path circuits becomes necessary. SpiceCut-Memory automatically builds the critical-path circuits to reduce simulation time - especially for characterization at multiple slew rates, multiple loadings and multiple PVTs. To characterize setup and hold time, only a small

critical-path circuit is needed with measurement nodes for simulation, and full-circuit may not help.

To further enhance the performance, an Asymptotic Waveform Evaluation (AWE)-based RC reduction has been built into SpiceCut. The critical coupling effects that are necessary for memory simulation are always taken into account.

Features of SpiceCut

- Build 'Critical-Path' Netlist
  - Create a small equivalent circuit for Spice simulation by removing the redundancy and remodeling memory arrays
  - Build bi-section models for setup / hold time and minimum clock width
  - Perform RC reduction
  - Generate critical-path circuits for power
- Verify and Debug Circuit
  - Verify memory structure from layout-extracted netlist.
  - Check the decoder function by toggling all address patterns, and simulating them
  - Locate worst and best word line by running Spice simulation on each pattern automatically
  - ERC analysis over entire chip

Locate Critical-Path of Memory Design

SpiceCut-Memory can exhaustively simulate all address patterns, automatically verify the corresponding wordline and measure the timing from address change to wordline's. The worst and best wordline can then be located, as shown below.

wadr0	wadr1	wadr2	wadr3	wadr4	wadr5	Word	Delay
0	0	0	0	0	0	F13712	1.80ns
1	0	0	0	0	0	F56432	1.82ns
	. . .						
1	1	1	1	1	1	F34577	1.94ns
Worst-Delay Wordline							
1	1	1	1	1	1	F34577	1.94ns
Best-Delay Wordline							
0	0	0	0	0	0	F13712	1.80ns

MemChar: Memory Characterization

MemChar incorporates multiple patented technologies that can automatically characterize the embedded memories and generate timing and power models at silicon-level accuracy. With increasing design complexity and rising clock frequencies, the reliability issues such as "glitches," and "metastability" are becoming critical and difficult to observe at the output. As a result, the chip may not meet performance targets and the silicon yield may be low.

MemChar can prevent reliability problems by setting up characterizations that determine the true setup and hold times.

Features of MemChar

- Generate the simulation stimulus and controls for all timing and power parameters.
- Control the creation of numerous Spice netlists along with the necessary measurement statements through running SpiceCut.
- Manage operations such as automating sweep loops for timing tables and optimization.
- Allow users to specify a preferred circuit simulator.
- Perform reliability checking - including glitch prevention and design margin checking.

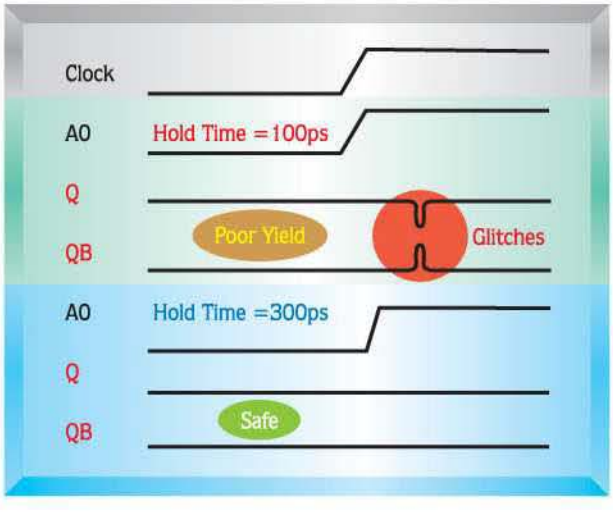
Complete Solution

- 'Bi-Section' Mode
  - Setup and hold time from binary iterations
  - Glitches and racing prevention
  - Accurate and automated
- 'Path-difference' Mode
  - Setup/hold time from paths' difference
  - Automated by latch pattern recognition

'Glitch' Prevention for Improving Yield

The ill effects of glitches are often realized too late. They directly impact the reliability and the performance - especially in memory circuits. Since the glitches are embedded internally, they cannot be observed at output pins. This makes it extremely difficult to debug the error. SpiceCut and MemChar analyze the memory instance timing behaviour from the inside out and can determine optimized glitch-free timing values.

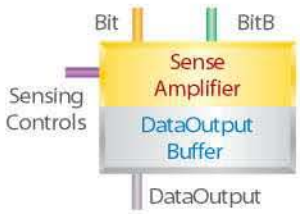
The example below shows that if the hold time is too short (100 ps), it will induce glitches in internal nodes of latches (Q and QB). With the true hold time (300 ps), it can prevent glitches from happening.



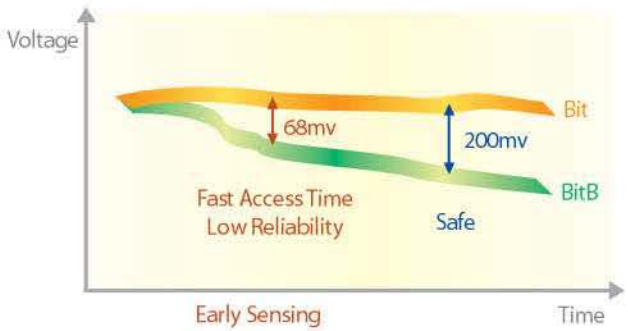
Margin Verification for Improving Yield

Sense amplifier input is the voltage difference of Bit and BitB and is sensed by a pulse signal. Internal noise can override the sensed signals if they are too small and cause false data outputs.

- Early sensing causes small V(Bit-BitB) and fast access time, and potential reliability issues.
- Late sensing causes large V(Bit-BitB) and slow access time, but with safer margins.



The change on process, power supply and temperature (PVT) will impact the reliability due to signal variations on Bit, BitB and Sensing Controls.



The Example of Verification Results

Design Margin	Sensing at	Access Time	V(Bit-BitB)
1000	7.477ns	4.3212ns	365.8mv
1101	5.977ns	2.8109ns	200.6mv
0111	5.040ns	1.8824ns	95.9mv
1111	4.790ns	1.6969ns	68.3mv

MSIM

MSIM is a matrix-inversion based circuit simulator with optimized algorithms to deliver unparalleled accuracy, performance and value.

Features of MSIM

- Accuracy : Within 1% compared to the current market leading SPICE simulator
- Speed : More than twice the speed compared to the current market leading SPICE simulator
- Optimization : Optimized for memory and standard cell characterization
- Price-Performance : Excellent value from a state of the art engine at a fraction of the cost

Parallel Running MSIM

For high throughput, multiple MSIM simulators can be concurrently run from CharFlo-Memory!. The benchmark results of 25 'access time' simulations (5 input slopes and 5 output loadings) on a medium-size register file are listed below

	CPU Time	Gains
1 MSIM	7 Hours 17 Minutes	1.0 X
4 MSIM	2 Hours 8 Minutes	3.4 X
8 MSIM	1 Hour 3 Minutes	6.0 X
25 MSIM	18 Minutes	23.9 X

The Platform and Support

- Commercial Memory Compiler Users
  - Artisan, Virage, TSMC, Faraday, Virtual Silicon, Dolphin Technology, Synopsys (Avanti), VeriSilicon, ...
- In-house Memory Compiler Development
  - Support designs with multiple ports, synchronous and asynchronous, and work with Ring-Shape extracted arrays.
- Major Memory Designs
  - Synchronous / Asynchronous
  - Single-port / Dual-port SRAM
  - Single-port / Dual-port Register File
  - ROM, ...
- Major Technologies
  - 0.25um, 0.18um, 0.15um, 0.13um, 90nm, ...
- Major Foundries
  - TSMC, UMC, IBM, Tower, ...
- Computer Operating System
  - Sun Solaris, Linux (RedHat 7.3 and higher)
- Simulation Job Controls
  - SunGrid and LSF

Summary

Legend Design Technology, Inc. provides SoC designers a complete characterization solution for embedded memory. With an emphasis on productivity and value, Legend's CharFlo-Memory! products - MSL, SpiceCut, MemChar and MSIM - automate the time consuming and error prone processes associated with characterization. MSL provides the controls for '.Lib-in and .Lib-out' memory instance characterization. By treating the extracted memory circuit as an entity from layout, SpiceCut accounts for all coupling, parasitics, and distributed effects when it builds optimized critical-path circuits. MemChar automates the characterization process by determining the stimuli, controls, and measurement statements needed for simulation. MSIM is a high accuracy circuit simulator offering excellent price-performance for both memory and standard cell characterization.

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