News Release

Legend releases Memory QA Solutions for on-chip memory IP instances

SANTA CLARA, Calif., September 22, 2015 – Legend Design Technology, Inc. released the memory QA solutions for on-chip memory IP instances in SoC designs. With its industry-proven memory validation and characterization technologies, Legend has provided both tool (i.e. Memory Diagnoser) and service to ensure the quality of post-layout function, instance model accuracy, signal integrity and noise margin, from the layout-extracted circuit including parasitic data.

For advanced technologies like 16nm/20nm/28nm, the on-chip memory QA has become increasingly necessary because of:

1. High risks due to the complex technology and design,
2. Serious impacts due to the high volume and short life cycle, and
3. Uncertainty of using the configurations not assessable in vendor's QA. It is impossible to test each of several hundred thousand instances in a memory compiler.

Normally, the customers care only that the limited number of memory IP instances on their own SoC design can work well, not the entire compiler. So, they need to have an "incoming" QA solution for on-chip memory IPs, which occupy most of chip areas.

The types of QA for on-chip memory IP can be categorized by:

1. Post-layout function validation
   For example, the shape of memory instance could be odd. The "long" shape memory may cause the loading on word line to be unexpectedly large, which could result in low driving power and read/write function failure.
2. Instance .Lib model validation
   For example, the insufficient setup/hold time/clock frequency could cause function failures or low yields.
3. Signal integrity and noise margin validation
   For example, the low sense-amp input could be overwritten by on-chip noise, which would result in low yields.

Legend provides both tool (i.e. Memory Diagnoser) and service for the quality assurance (QA) of those on-chip memory IP instances, with the following functions:

1. Structure Recognition and Database Preparation
   Based on Legend's patented technology, recognize the memory structure and critical nets from the layout-extracted circuit including parasitic data. Then, build the critical-path circuits to run circuit simulations.
2. Model QA

Validate the input .Lib model by its correspondent stimulus and conditions through running simulations. If the failures are due to those insufficient setup and hold time, then find the optimized values iteratively.

3. Post-layout Function QA
   Validate the function of "access time" by simulating the critical-path circuits with the actual loadings extracted from layout. In case of a failure, examine the driving power such as the pulse width on word line signals.
4. Signal Integrity and Noise Margin QA
   Validate the signal integrity issues such as glitch and meta-stability, and perform the noise margin check on those easy-to-break signals such as sense-amplifier input. By sweeping EMA/RM margin pins, an exhaustive margin report of pin setting, V(bit-bitb), and access time will be generated.

Since memory IP instance is a "black box" to SoC designers, an incoming QA becomes very necessary to ensure the quality. Especially nowadays, the high risks from technology complexity and business impacts can be prohibitively unaffordable for those expensive SoC design projects. Legend's QA products and services for on-chip memory IP can look inside the memory circuits and validate those easy-to-break spots by using its patented technology and proprietary algorithms. Legend's solution has made it possible that incoming QA on memory IP instances can be done by customers.