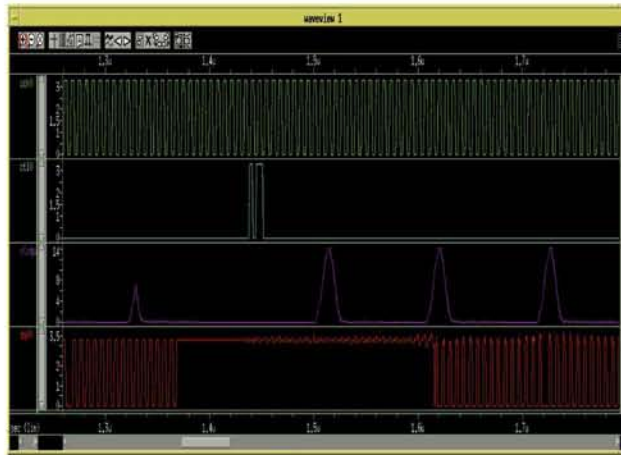


Turbo-MSIM™

High-Speed and High-Capacity Circuit Simulator



Turbo-MSIM™ Full-Chip Simulation Waveforms for a Mixed-Mode LCD Display Controller with Multi-Million MOSFETS

Highlights

- Super high speed
- Extremely large capacity
- Exceptional accuracy
- Broad model support
 - Leakage current model
 - High voltage model
 - Foundry models
 - Nanometer technology
- Built-in RC reduction
- Excellent price-performance

Turbo-MSIM is a high-speed and high-capacity circuit simulator with SPICE-like accuracy. Turbo-MSIM is ideal for full-chip circuit simulations.

Benefits

- **Accelerated simulation speed**
Simulation speed is orders of magnitude faster than conventional Spice simulators.
- **Full-chip simulation capacity**
Efficiently simulates full-chip designs, either hierarchical or flattened netlists.
- **Exceptional accuracy**
Turbo-MSIM uses optimized time-based algorithms and proven models to deliver silicon-accurate results.
- **Scalable speed, capacity and accuracy**
Achieves best-in-class throughput with scalable speed, capacity and accuracy.
- **Ultimate post-layout analysis**
Enables speedy post-layout simulation and includes state-of-the-art RC reduction.

Applications

- **Full-chip simulations for SoC designs**
Provides the capacity for full-chip simulation, either hierarchical circuit or flattened layout-extracted netlist.
- **Functional verification**
Supports transistor-level functional verification,

with vector input stimulus and vector output verification (VEC and VCD).

- **Timing and power analysis**
Performs transient analysis for timing verification and accurate power simulation, especially for leakage power. Turbo-MSIM is extraordinarily accurate for circuits with multiple voltage sources.
- **Memory and mixed-mode designs**
Proficiently recognizes repeated structures in memory circuits to optimize simulation throughput. Incorporates advanced algorithms and interfaces for mixed-mode designs.

Features

- **Tabular device models for speed-up**
Generates tabular device models from complicated analytical models. Table-lookup models facilitate much faster simulation speed.
- **Latency detection for throughput**
Simulates only active circuits by latency detection to dramatically enhance speed.
- **Subcircuits and hierarchy rebuilding**
Extracts sub-circuits and re-build hierarchy from flattened circuit for speed and memory efficiency.
- **Advanced RC reduction**
Built-in RC reduction modules are used to enhance the performance by reducing the size of circuit matrix during DC and transient iterations.

Benchmark Results

1. Speed, Capacity and Accuracy Benchmark

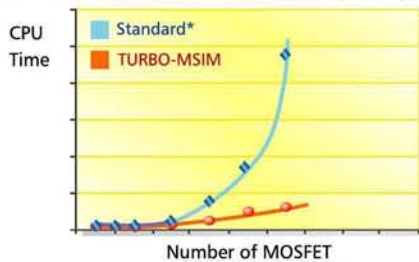
'Access time' simulations on a 0.13um high-speed SRAM circuits with MOSFET counts ranging from 31,741 to 6,395,298. If taking HSPICE (accurate mode) as the gold, the difference of Turbo-MSIM (accurate mode) is less than 0.5% and the difference of Turbo-MSIM (default mode) is less than 1.5%.

Circuit Type	MOS Count	Spice CPU Time	Turbo-MSIM CPU Time	Turbo-MSIM Speed Up	Accuracy Difference
Circuit 1	31,741	11,707 sec	37 sec	316 X	0.66 %
Circuit 2	57,079	21,483 sec	46 sec	467 X	1.50 %
Circuit 3	110,567	73,355 sec	78 sec	940 X	0.37 %
Circuit 4	1,619,735	N/A	756 sec	N/A	N/A
Circuit 5	3,198,065	N/A	1,636 sec	N/A	N/A
Circuit 6	6,395,298	N/A	5,725 sec	N/A	N/A

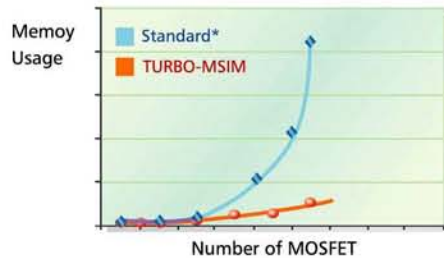
2. Performance Benchmark

Simulations have been run on different size circuits with the following results

- Turbo-MSIM is exponentially faster than the Standard*

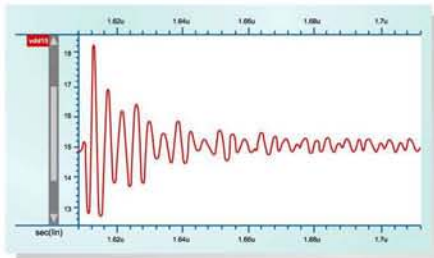


- Turbo-MSIM uses exponentially smaller memory than the Standard*



* Standard means the most popular Spice simulator

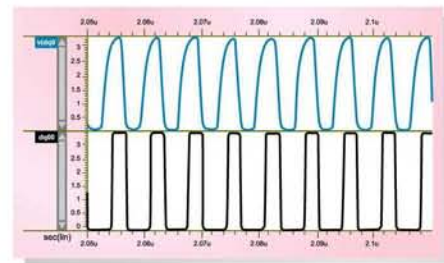
3. Ground Bounce Simulation Benchmark



Turbo-MSIM performs full-chip simulation and is used to analyze ground bounce effects with superior accuracy. This helps minimize the risk associated with ground bounce on real silicon.

4. Full-chip Functional Verification

Turbo-MSIM performs transistor-level full-chip simulation to verify the results with the expected outputs in vector form. The comparison between simulation results and expected output vectors are shown below



Specification

Design Inputs

- SPICE netlist
- HSPICE™ compatible netlist

Device Models

- MOSFET models, including BSIM3 and BSIM4 models
- Bipolar junction transistor (BJT) models
- Diode models
- Unified and compact capacitance models
- Charge conservation and high voltage models

Design Outputs

- WDF Waveform format
- FSDB Waveform format
- HSPICE™ compatible Waveform and Measurement format
- ASCII text

Platforms

Sun Solaris, HP-UX and Linux (RedHat 7.3 and higher)

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