USB3.0 Channel Simulation

Schematic

USB channel schematics with cable

Test circuit

**Input Signal Source**  **Cable**  **CTLE (Continuous Time Linear Equalizer)**
USB3.0 Channel Simulation

Components

♦ Input Signal: PRBS

Voutp inp 0 PWL(
+ 0.00000000e+000 -0.800000
+ 3.00000000e-011 0.800000
+ 2.00000000e-010 0.800000
+ 2.30000000e-010 -0.800000
...

♦ Cable: 4-port transmission line Macro-model

xcable inp inn n3 n4 skewcable3m_passive
.subckt skewcable3m_passive a_1 a_2 a_3 a_4
VI_1 a_1 NI_1 0
RI_1 NI_1 ref 5.0000000000000000e+001
GC_1_1 ref NI_1 NS_1 0 -1.6802855942555286e+001
...
.ends

Legend

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**Components**

- **CTLE:** Continuous Time Linear Equalizer

  E1 0 outn Laplace 0 n4 2.5659E+20 6.286E+10 /
  3.845244E+20 4.3646E+10 1.0

It acts as a High-Pass filter at 750MHz, then acts as a gain Amplifier at 750MHz to 7.5GHz, then acts as a Low-Pass filter at over 7.5GHz to compensate Cable Loss.

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MSIM-PCB Simulation Results

Input Signal

Output Signal
USB3.0 Channel Simulation

Eye-Diagram

Eye Diagram

Eye Width (UI): 400 p sec
Trigger Period: 0.5 UI

Verification Standards:

... Minimum eye height
Minimum eye width
...
MSIM® Certifications

◆ JEITA (Japan Electric and Information Technology Industries Association) has qualified MSIM-PCB for simulating IBIS models in PCB designs. Those results can be downloaded from JEITA web:

https://ec.jeita.or.jp/ibis/

◆ MSIM certified by TSMC’s Spice Tool Qualification Program

http://www.legenddesign.com/BW/021009.shtml